WHAT IS CLAIMED IS:

1. A ferroelectric memory comprising:

a plurality of memory cells respectively including ferroelectric capacitors and switch transistors; and

the ferroelectric memory operating in a test mode in which, after polarized data is written into the memory cells by applying a first electric potential difference between both electrodes of the respective ferroelectric capacitors of the plurality of memory cells, and before reading of the polarized data from the memory cells is carried out, a second electric potential difference smaller than the first electric potential difference is applied between both the electrodes of the ferroelectric capacitors in a direction opposite to that at the time of writing the polarized data.

2. A ferroelectric memory according to claim 1, wherein the first electric potential difference is larger than an absolute value of a coercive voltage on a polarization hysteresis characteristic curve which the ferroelectric capacitors have.

3. A ferroelectric memory according to claim 1, wherein the second electric potential difference has an absolute value smaller than a coercive voltage on a polarization hysteresis characteristic curve which the ferroelectric capacitors have.

4. A ferroelectric memory according to claim 2,

wherein the second electric potential difference has an absolute value smaller than the coercive voltage.

5. A ferroelectric memory according to claim 1, wherein the second electric potential difference is applied plural times consecutively between both the electrodes of the ferroelectrode capacitor.

6. A ferroelectric memory according to claim 4, wherein the second electric potential difference is applied plural times consecutively between both the electrodes of the ferroelectrode capacitor.

7. A ferroelectric memory according to claim 1, wherein a third electric potential difference having an absolute value larger than the second electric potential difference is applied between both the electrodes of the ferroelectrode capacitor when reading of the polarized data from the memory cell is carried out.

8. A ferroelectric memory according to claim 5, wherein a third electric potential difference having an absolute value larger than the second electric potential difference is applied between both the electrodes of the ferroelectrode capacitor when reading of the polarized data from the memory cell is carried out.

9. A ferroelectric memory according to claim 6, wherein a third electric potential difference having an absolute value larger than the second electric

potential difference is applied between both the electrodes of the ferroelectrode capacitor when reading of the polarized data from the memory cell is carried out.

10. A ferroelectric memory according to claim 7, wherein the first electric potential difference and the third electric potential difference are equivalent.

11. A ferroelectric memory according to claim 1, wherein a circuit which generates the second electric potential difference is formed on a semiconductor chip along with the plurality of memory cells.

12. A ferroelectric memory according to claim 1, wherein one side electric current ends of the switch transistors are connected to one side electrodes of the ferroelectric capacitors of said plurality of memory cells, plate lines are connected to the other side electrodes of the ferroelectric capacitors, bit lines are connected to the other side electric current ends of the switch transistors, and word lines are connected to gate terminals of the switch transistors.

13. A ferroelectric memory according to any one of claim 1, wherein the ferroelectric capacitors in said plurality of memory cells are connected in series, said plurality of memory cells are connected in series due to the one side electrodes and the other side electrodes of the respective switch transistors in said plurality of the memory cells being connected in

parallel to the ferroelectric capacitors in the corresponding memory cells, plate lines are connected to the one side ends of said plurality of serially-connected memory cells, bit lines are connected to the other side ends of said plurality of serially-connected memory cells, and word lines are connected to gate terminals of the respective switch transistors.

14. A ferroelectric memory according to claim 1, wherein the test mode is an operation mode which is carried out after an initial data pattern is written into said plurality of memory cells, and an opposite pattern having a pattern opposite to the initial data pattern is written into said plurality of memory cells and before the opposite data pattern is read out.

15. A ferroelectric memory comprising:

a plurality of memory cells respectively including ferroelectric capacitors and switch transistors; and

the ferroelectric memory operating in a test mode in which, after polarized data is written into the respective memory cells by applying a first electric potential difference between both electrodes of ferroelectric capacitors of said plurality of memory cells, and before reading of the polarized data from the memory cells is carried out, a second electric potential difference is applied between both the electrodes of the ferroelectric capacitors so as to weaken polarization.

16. A ferroelectric memory according to claim 15, wherein the second electric potential difference has an absolute value which is smaller than a coercive voltage on a polarization hysteresis characteristic curve which the ferroelectric capacitors have.

17. A method of testing a ferroelectric memory having a plurality of memory cells each including a ferroelectric capacitor and a switch transistor, comprising:

writing polarized data into the memory cells by applying a first electric potential difference between both electrodes of the ferroelectric capacitors of said plurality of memory cells;

weakening polarization of the ferroelectric capacitors by applying a second electric potential difference smaller than the first electric potential difference between both the electrodes of the ferroelectric capacitor of the corresponding memory cell in a direction opposite to that at the time of writing the polarized data; and

reading the polarized data.

18. A method according to claim 17, wherein the second electric potential difference has an absolute value smaller than a coercive voltage on a polarization hysteresis characteristic curve which the ferroelectric capacitors have.

19. A method according to claim 17, wherein the

second electric potential difference is applied plural times consecutively between both the electrodes of the ferroelectrode capacitor.

20. A method according to claim 17, wherein a third electric potential difference larger than the second electric potential difference is applied between both the electrodes of the ferroelectrode capacitor when reading of the polarized data from the memory cell is carried out.

21. A method according to claim 17, wherein, when the polarized data is written into the memory cell by applying the first electric potential difference between both the electrodes of the respective ferroelectric capacitors of said plurality of memory cells, an electric potential difference whose absolute value is larger than a coercive voltage on a polarization hysteresis characteristic curve which the ferroelectric capacitor has is applied as the first electric potential difference.

22. A method according to claim 20, wherein the first electric potential difference and the third electric potential difference are equivalent.

23. A method according to claim 17, wherein, when polarized data is written into the memory cell by applying the first electric potential difference between both the electrodes of the respective ferroelectric capacitors of said plurality of memory

cells, an initial data pattern is written into said plurality of memory cells in advance, and an opposite data pattern having a pattern opposite to the initial data pattern is written into said plurality of memory cells.